Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously Presented) A method for fabricating a shallow trench isolation region, comprising:

forming an intermediate layer upon an upper surface of a semiconductor topography, wherein the intermediate layer comprises a doped oxide layer;

forming one or more trenches within the intermediate layer and the semiconductor topography;

blanket depositing a trench fill material over and within the one or more trenches;

polishing the trench fill material with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form an upper surface at an elevation above the trenches, wherein the upper surface does not comprise a polish stop material; and

etching an entirety of the upper surface simultaneously, wherein remaining portions of the trench fill material are laterally confined within the trenches.

2. (Original) The method of claim 1, wherein an upper surface of the remaining portions is above an upper surface of a semiconductor substrate within the semiconductor topography.

3. (Original) The method of claim 2, wherein said upper surface of the remaining portions is less than approximately 200 angstroms above the upper surface of the semiconductor substrate.

4. (Previously Presented) The method of claim 1, wherein the step of polishing comprises inserting a fluid consisting essentially of water between the trench fill material and the abrasive polishing surface.

5. (Previously Presented) The method of claim 1, wherein said etching comprises etching at least a portion of the doped oxide layer.

6. (Previously Presented) The method of claim 1, wherein said intermediate layer further comprises a base oxide layer.

7. (Canceled)

8. (Previously Presented) The method of claim 1, wherein said doped oxide layer comprises borophosphosilicate glass.

9. (Previously Presented) The method of claim 1, wherein said intermediate layer further comprises a nitride layer, and wherein a thickness of said nitride layer is less than approximately 500 angstroms.

10. – 11. (Canceled)

12. (Previously Presented) A method for processing a semiconductor topography, comprising:

polishing an upper layer of said semiconductor topography with an abrasive polishing surface in the presence of a fluid that is substantially free of particulate matter to form an upper surface of the semiconductor topography at an elevation above an underlying layer, wherein the underlying layer comprises a lateral variation in polishing characteristics, and wherein the step of polishing comprises inserting a fluid consisting essentially of water between the semiconductor topography and the abrasive polishing surface; and

etching the entirety of the upper surface of the semiconductor topography simultaneously to expose the underlying layer.

13. (Original) The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid dishing during said polishing.

14. (Original) The method of claim 12, wherein said upper surface of the semiconductor topography is spaced sufficiently above the underlying layer to avoid polishing the underlying layer.

15. (Original) The method of claim 12, wherein said elevation is between approximately 100 angstroms and approximately 1000 angstroms.

16. (Canceled)

17. (Original) The method of claim 12, wherein said upper layer comprises an interlevel dielectric layer.

18. (Original) The method of claim 17, wherein said interlevel dielectric layer comprises silicon dioxide.

19. (Original) The method of claim 12, wherein said underlying layer comprises a silicon substrate patterned with dielectric filled trenches.

20. – 30. (Canceled)

31. (Previously Presented) The method of claim 12, further comprising:

forming an intermediate layer upon an upper surface of the semiconductor topography;

forming one or more trenches within the intermediate layer and the semiconductor topography; and

blanket depositing the upper layer over and within the one or more trenches prior to the step of polishing the upper layer.

32. (Previously Presented) The method of claim 31, wherein the intermediate layer comprises a doped oxide layer.

33. (Previously Presented) The method of claim 32, wherein said doped oxide layer comprises borophosphosilicate glass.

34. (Previously Presented) The method of claim 31, wherein said intermediate layer comprises a nitride layer with a thickness of less than approximately 500 angstroms.

35. (Previously Presented) The method of claim 31, wherein said intermediate layer further comprises a silicon carbide layer.

36. (Previously Presented) The method of claim 31, wherein said intermediate layer further comprises a carbonated polymer layer.

37. (New) A method for fabricating a shallow trench isolation region, comprising:

forming an oxide layer upon and in contact with a substrate comprising silicon;

forming one or more trenches within the oxide layer and the substrate;

blanket depositing a fill material within the one or more trenches and upon and in contact with remaining portions of the oxide layer;

polishing the fill material with an abrasive polishing surface in the absence of a fluid or in the presence of a fluid that is substantially free of particulate matter to form a substantially planar surface at an elevation above an uppermost surface of the substrate; and

etching an entirety of the substantially planar surface simultaneously to expose the substrate.

38. (New) The method of claim 37, wherein the step of forming the oxide layer comprises growing the oxide layer by thermal oxidation of the substrate.

39. (New) The method of claim 37, wherein the step of forming the oxide layer comprises depositing the oxide layer by chemical vapor deposition techniques.

40. (New) The method of claim 37, wherein the oxide layer consists essentially of silicon oxide.

41. (New) The method of claim 37, wherein the oxide layer consists essentially of siliconoxynitride.

42. (New) The method of claim 37, wherein said elevation is between approximately 100 angstroms and approximately 1000 angstroms above the uppermost surface of the substrate.

43. (New) The method of claim 37, wherein the step of forming the oxide layer comprises forming the oxide layer to have a thickness between approximately 50 angstroms and approximately 250 angstroms.

44. (New) The method of claim 37, wherein the step of polishing comprises inserting a fluid consisting essentially of water between the fill material and the abrasive polishing surface.

45. (New) The method of claim 37, wherein the step of polishing comprises polishing at least a portion of the oxide layer.